REMARKS

Applicants have provided a new Title of the Invention as required by the Examiner.

Claims 13 and 14 have been amended to overcome the 35 USC 112, second paragraph rejection.

According to the office action, claims 1, 5-6, 26 and 30-31 under 35 U.S.C. § 102(e) are rejected as being anticipated by Sharma et al '463; claims 7 and 34 are rejected as being anticipated by Luick '362; claims 8, 10-11, 35 and 37-38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Luick '362; claims 12 and 39 are rejected as being unpatentable over Luick as applied to claim 8 and 35 and further in view of Richter et al '885; claims 13 and 14 are rejected as being unpatentable over Kenzo in view of Richter; claims 15 and 32 are rejected over Luick in view of Richter; and claims 22-24 are rejected over Sharma in view of Kenzo. reconsideration of these rejections is requested in view of the foregoing amendments and for the following reasons.

Independent claims 1, 7, 26 and 34 have each been amended to include the limitation wherein the external device control information is an information which specifies at least one of an access timing, a memory attribute, and a bus width of the device. This limitation is set forth in original claim 2, for example, which has been indicated as being allowable if

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rewritten in independent form. Accordingly, claims 1-12, 26-31 and 34, 35 and 37-39 should be found allowable in view of the amendments to claims 1, 7, 26 and 34.

Conventionally, translating a virtual address used for accessing an external device into an external memory address is employed by using a translation look-aside buffer (TLB). According to the present invention, external device control information that designates a method of accessing an external device having an interface, such as a PCMCIA interface, is stored in the TLB provided in a data processor. This aspect of the invention is set forth in claim 13. In claim 14, the data processing system further sets forth that the address necessary to access the device by the address translation buffer at the time of accessing the device is translated and the device is controlled by the data processor in accordance with the control information that is kept in the address translation buffer. Accordingly, claims 13 and 14 are patentable over Kenzo in view of Richter.
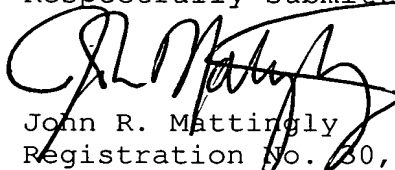
In claim 15, the address translation means is claimed as storing external device control information for controlling the external device, which has an PCMCIA interface. The external device control information is stored in association with one of a first address output by the CPU or a second address translated by the address translation means. Claim 32

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is similar to claim 15 and each of these claims is patentable

over Luick in view of Richter. Accordingly, the 35 USC 103(a)

rejection of claims 15 and 32 should be withdrawn.

Claim 22 sets forth a data processor with first and

second address translation means that translates a virtual

address to a physical address and outputs the physical

address. The first and second address translation means

stores an external device control information for controlling

the external device in association with either the first or

second address. Either the external device control

information from the first address translation means or the

second address translation means is selected and output to the

external bus control means which provides an output to the

external device. Accordingly, claims 22-24 are patentable

over Sharma in view of Kenzo.

In view of the foregoing amendments and remarks,

reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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